What is claimed is:

[Claim 1] 1. A method of forming a circuit, comprising the steps of:

forming a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation;

forming, separately, an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation; and

superimposing the upper semiconductor device on the lower semiconductor device.

[Claim 2] 2. The method of claim 1, wherein the first crystal orientation is different from the second crystal orientation.

[Claim 3] 3. The method of claim 1, further comprising forming at least one layer of semiconductor device between the lower and upper semiconductor devices.

[Claim 4] 4. The method of claim 1, further comprising bonding the upper semiconductor device to the top of the lower semiconductor device with an insulating layer.

[Claim 5] 5. The method of claim 4, further comprising electrically connecting at least a portion of the upper semiconductor device to at least a portion of the lower semiconductor device.

[Claim 6] 6. The method of claim 1, further comprising forming the lower semiconductor as a pFET device and forming the upper semiconductor as an nFET device.

[Claim 7] 7. The method of claim 6, further comprising forming an active region of the pFET device in a crystal orientation of [100] and forming an active region of the nFET device in a crystal orientation of [110].

[Claim 8] 8. A method of forming an inverter, comprising the steps of:

forming a lower semiconductor layer comprising a first crystal orientation;

forming at least one lower source/drain region in the lower semiconductor layer;

forming a lower gate on the lower semiconductor layer to define an active region in the lower semiconductor layer;

forming an upper semiconductor layer comprising a second crystal orientation;

forming at least one upper source/drain region in the upper semiconductor layer;

forming an upper gate on the upper semiconductor layer to define an active region in the upper semiconductor layer;

bonding the upper semiconductor layer to the lower semiconductor layer; and

electrically connecting the at least one lower source/drain region to the at least one upper source/drain region.

[Claim 9] 9. The method of claim 8, further comprising forming the first crystal orientation as [100] and forming the second crystal orientation as [110].

[Claim 10] 10. The method of claim 9, further comprising electrically connecting the at least one lower source/drain region to the at least one upper source/drain region with metal plugs.

[Claim 11] 11. The method of claim 8, further comprising forming the lower semiconductor layer as a pFET device, and forming the upper semiconductor layer as an nFET device.

[Claim 12] 12. The method of claim 8, further comprising bonding the upper semiconductor layer to the lower semiconductor layer with an insulator.

[Claim 13] 13. The method of claim 8, further comprising bonding the upper semiconductor layer to the lower semiconductor layer with SiO_2.

[Claim 14] 14. A circuit, comprising:

a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation; and

an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation, wherein the upper semiconductor device is formed separately from the lower semiconductor device and connected thereto by an interconnect structure.

[Claim 15] 15. The circuit of claim 14, wherein the first crystal orientation is different from the second crystal orientation.

[Claim 16] 16. The circuit of claim 14, further comprising at least one layer of a semiconductor device between the lower and upper semiconductor devices.

[Claim 17] 17. The circuit of claim 16, wherein at least one semiconductor device of the at least one layer of semiconductor device comprises an active region having a crystal orientation different from the crystal orientation of at least any one of the lower semiconductor device and the upper semiconductor device.

[Claim 18] 18. The circuit of claim 14, wherein the upper semiconductor device is bonded to the top of the lower semiconductor device with an insulating layer, and wherein at least a portion of the upper semiconductor device is electrically connected to at least a portion of the lower semiconductor device.

[Claim 19] 19. The circuit of claim 18, wherein:

the lower semiconductor device includes either a pFET device or an nFET device, and the upper semiconductor device includes either a pFET device or an nFET device; and

the crystal orientation of the active region of the respective lower semiconductor device is different from the crystal orientation of the active region of the respective upper semiconductor device.

[Claim 20] 20. The circuit of claim 18, wherein the lower and upper semiconductor devices comprise an inverter, and the pFET device has a crystal orientation of [100] in an active region and the nFET device has a crystal orientation of [110] in an active region.